```
primitive simple_dff (Q, D, CLK, SET);
    output Q;
    input  D, CLK, SET;
    reg    Q;

    // Positive edge triggered D flip-flop with active high
    // asynchronous set

    table
    //  D     CLK    SET      Q       Q+

        1     (01)   0   :   ?   :   1; // line 1: clocked data
        0     (01)   0   :   ?   :   0; // line 2: clocked data

        ?      ?     *   :   ?   :   1; // line 3: ignore: pessimism

        ?      ?     1   :   ?   :   1; // line 4: asynchronous set

        ?    (?0)    ?   :   ?   :   -; // line 5: ignore falling clock

        *      1     ?   :   ?   :   -; // line 6: ignore data edges
        *      0     ?   :   ?   :   -; // line 7: ignore data edges

    endtable
endprimitive
```

FIG. 1

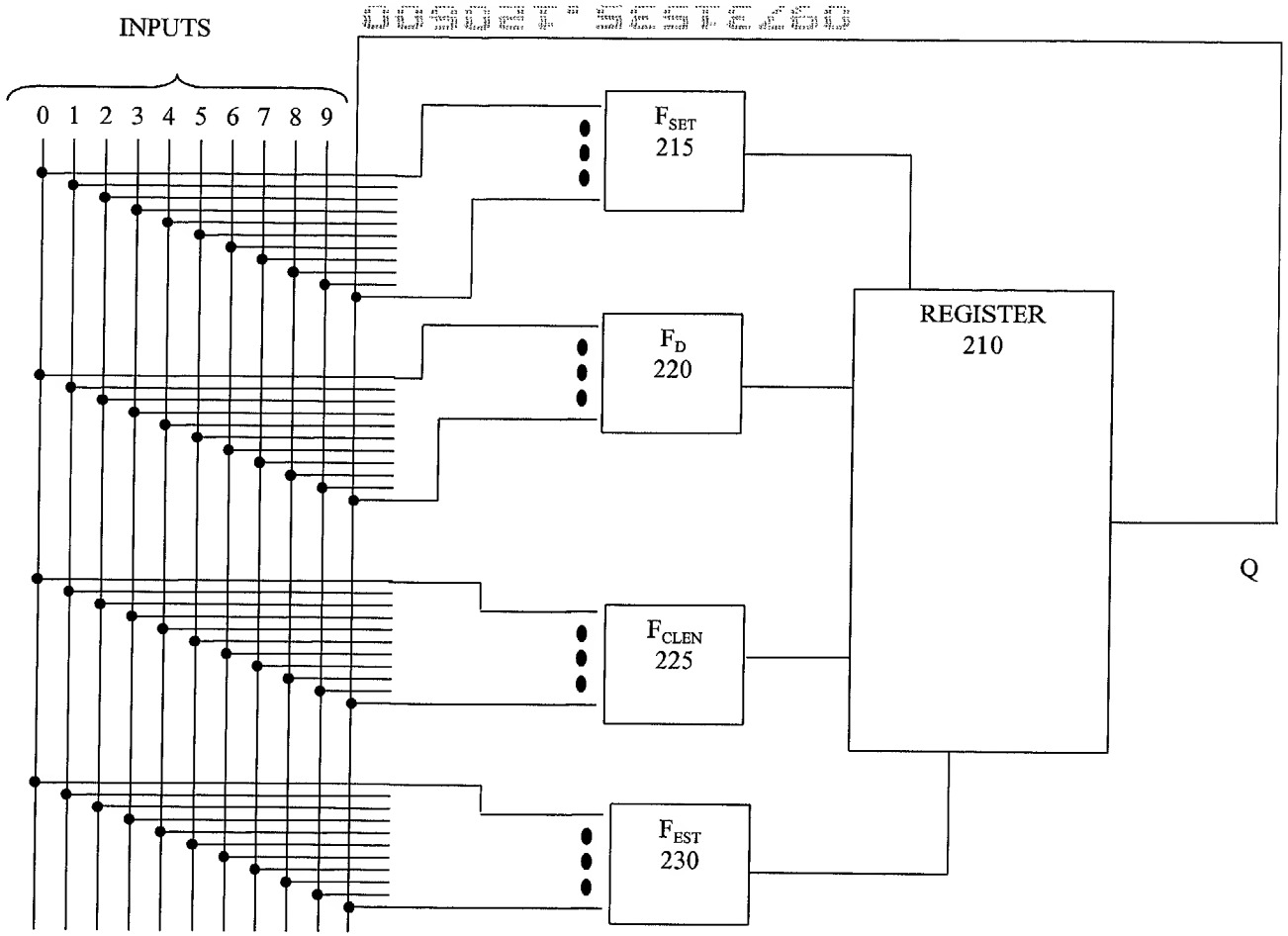
INPUTS
0 1 2 3 4 5 6 7 8 9
F_{SET} 215
F_D 220
F_{CLEN} 225
F_{EST} 230
REGISTER 210
Q

FIG. 2

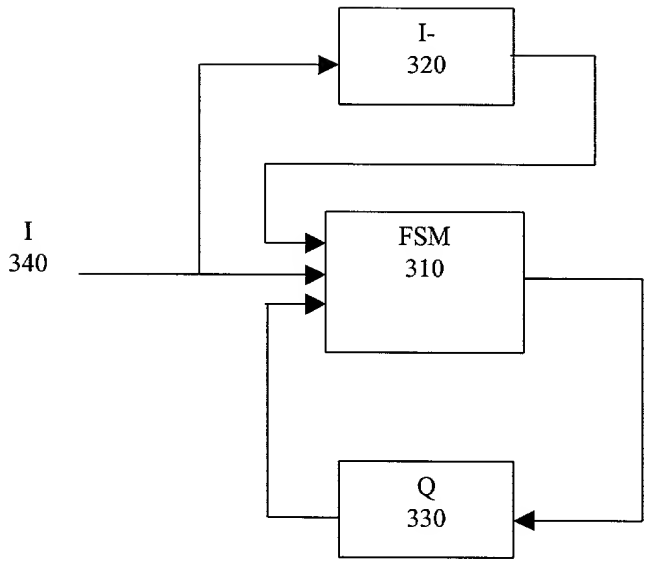

FIG. 3

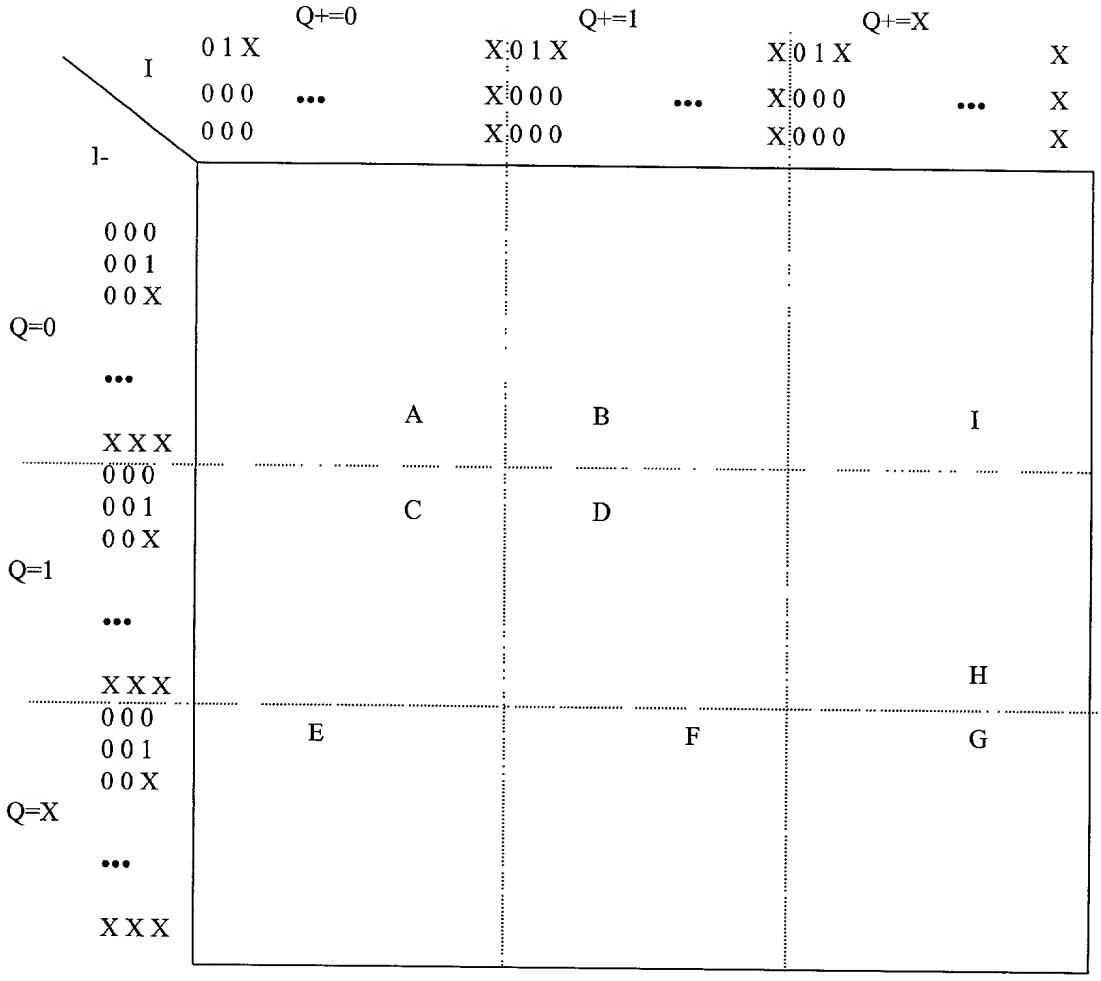
Q+=0
Q+=1
Q+=X
I
01X
000
000
X01X
X000
X000
X01X
X000
X000
X
X
X
l-
000
001
00X
Q=0
•••
XXX
000
001
00X
Q=1
•••
XXX
000
001
00X
Q=X
•••
XXX
A
B
I
C
D
H
E
F
G

FIG. 4

```
     0-00000000000000000001111111111111111111XXXXXXXXXXXXXXXXXXX
     1-00000001111111XXXXX00000001111111XXXXX00000001111111XXXXX
     2-0001XXX0001XXX001XX0001XXX0001XXX001XX0001XXX0001XXX001XX
     3-01X101X01X101X1X11X01X101X01X101X1X11X01X101X01X101X1X11X
0123  ------------------------------------------------------------
0000:R:...L.E.E.......A...E..................E.................
0001:R:...L.E.E.......A....E..................E................
000X:R:...L.E.E.......A.....E..................E...............
0010:U:.E...E....L.....L.....L..................L...............
0011:R:.E...E....L.....L.....L..................L...............
001X:U:.E...E....L.....L.....L..................L...............
00X0:U:.E.L.........A....A....E..................E..............
00X1:R:.E.L.........A....A.....E..................E.............
00XX:R:.E.L.........A....A......E..................E............
0100:R:E.........L.E..A..........E..................E...........
0101:R:.E........L.E..A...........E..................E..........
010X:R:..E.......L.E..A............E..................E.........
0110:U:...L....E...E...L............L..................L........
0111:R:...L....E...E...L............L..................L........
011X:U:...L....E...E...L............L..................L........
01X0:U:....E...E.L.......A...........E..................E.......
01X1:R:.....E..E.L.......A............E..................E......
01XX:R:......E.E.L.......A.............E..................E.....
0X00:U:E........A......LE...............A..................A...
0X01:R:.E.......A......LE...............A..................A...
0X0X:R:..E......A......LE...............A..................A...
0X10:U:...L......L...E..E................L..................L..
0X11:R:...L......L...E..E................L..................L..
0X1X:U:...L......L...E..E................L..................L..
0XX0:U:....E........AE.L....................A..................A
0XX1:R:.....E.......AE.L....................A..................A
0XXX:R:......E......AE.L....................A..................A
1000:R:E.....................L.E..E......A...E..................
1001:R:.E....................L.E..E......A....E.................
100X:R:..E...................L.E..E......A.....E................
1010:U:...L................E...E....L.....L.....L..............
1011:R:...L................E...E....L.....L.....L..............
101X:U:...L................E...E....L.....L.....L..............
10X0:U:....E..............E.L.........A....A....E.............
10X1:R:.....E.............E.L.........A....A.....E............
10XX:R:......E............E.L.........A....A......E...........
1100:R:.......E...........E.........L.E..A..........E..........
1101:R:........E..........E........L.E..A...........E.........
110X:R:.........E..........E.......L.E..A............E........
1110:U:..........L..........L....E...E...L............L.......
1111:R:..........L..........L....E...E...L............L.......
```

FIG. 5A

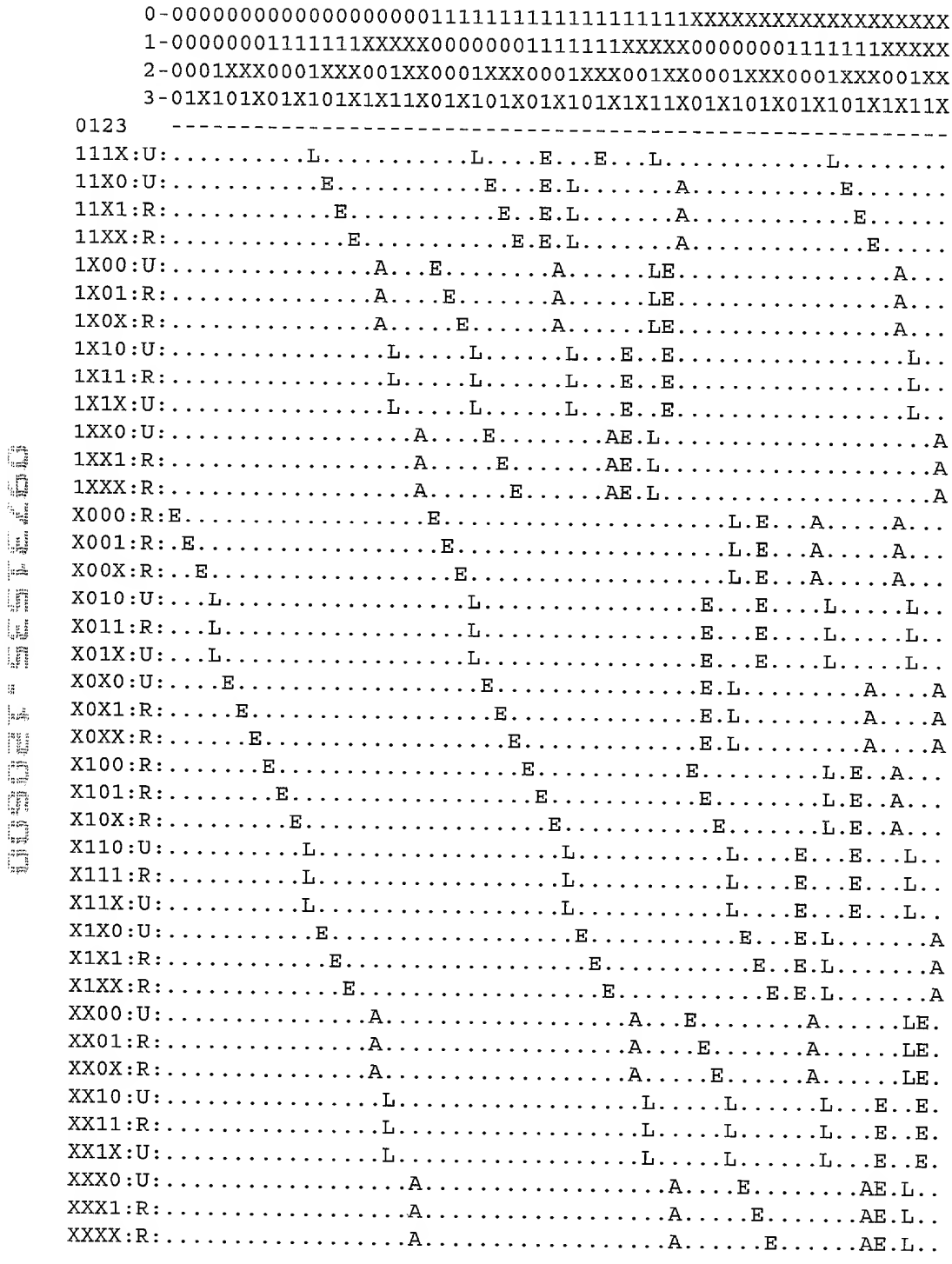
0-00000000000000000001111111111111111111XXXXXXXXXXXXXXXXXXXX
1-00000001111111XXXXX00000001111111XXXXX00000001111111XXXXX
2-0001XXX0001XXX001XX0001XXX0001XXX001XX0001XXX0001XXX001XX
3-01X101X01X101X1X11X01X101X01X101X1X11X01X101X01X101X1X11X
0123
111X:U:.....L.....L....E...E...L.....L.....
11X0:U:.....E.....E...E.L.....A.....E.....
11X1:R:.....E.....E..E.L.....A.....E.....
11XX:R:.....E.....E.E.L.....A.....E.....
1X00:U:.....A...E.....A.....LE.....A...
1X01:R:.....A....E.....A.....LE.....A...
1X0X:R:.....A.....E.....A.....LE.....A...
1X10:U:.....L.....L.....L...E..E.....L..
1X11:R:.....L.....L.....L...E..E.....L..
1X1X:U:.....L.....L.....L...E..E.....L..
1XX0:U:.....A....E.....AE.L.....A
1XX1:R:.....A.....E.....AE.L.....A
1XXX:R:.....A.....E.....AE.L.....A
X000:R:E.....E.....L.E...A.....A...
X001:R:.E.....E.....L.E...A.....A...
X00X:R:..E.....E.....L.E...A.....A...
X010:U:...L.....L.....E...E....L.....L..
X011:R:...L.....L.....E...E....L.....L..
X01X:U:...L.....L.....E...E....L.....L..
X0X0:U:....E.....E.....E.L.....A....A
X0X1:R:.....E.....E.....E.L.....A....A
X0XX:R:.....E.....E.....E.L.....A....A
X100:R:.....E.....E.....E.....L.E..A...
X101:R:.....E.....E.....E.....L.E..A...
X10X:R:.....E.....E.....E.....L.E..A...
X110:U:.....L.....L.....L....E...E...L..
X111:R:.....L.....L.....L....E...E...L..
X11X:U:.....L.....L.....L....E...E...L..
X1X0:U:.....E.....E.....E...E.L.....A
X1X1:R:.....E.....E.....E..E.L.....A
X1XX:R:.....E.....E.....E.E.L.....A
XX00:U:.....A.....A...E.....A.....LE.
XX01:R:.....A.....A....E.....A.....LE.
XX0X:R:.....A.....A.....E.....A.....LE.
XX10:U:.....L.....L.....L.....L...E..E.
XX11:R:.....L.....L.....L.....L...E..E.
XX1X:U:.....L.....L.....L.....L...E..E.
XXX0:U:.....A.....A....E.....AE.L..
XXX1:R:.....A.....A.....E.....AE.L..
XXXX:R:.....A.....A.....E.....AE.L..

FIG. 5B

	I, Q +	0001	0011	00X1	0101	0111	01X1	0X01	0X11	0XX1	1001	1011	10X1	1101	1111	11X1	1X01	1X11	1XX1	X001	X011	X0X1	X101	X111	X1X1	XX01	XX11	XXX1
I -, Q																												
0001	R		L	E							E									E								
0011	R	E		E		L			L			L									L								
00X1	R	E	L										E									E							
0101	R	E				L	E							E									E						
0111	R		L		E		E		L						L									L					
01X1	R			E	E	L										E									E				
0X01	R	E							L	E																			
0X11	R		L					E		E									L										L
0XX1	R			E				E	L																				
1001	R	E										L	E	E						E									
1011	R		L								E		E		L			L			L								
10X1	R			E							E	L										E							
1101	R				E						E				L	E							E						
1111	R					L						L		E		E		L						L					
11X1	R						E						E	E	L							E							
1X01	R										E							L	E										
1X11	R								L			L			L		E		E										L
1XX1	R												E				E	L											
X001	R	E									E										L	E							
X011	R		L									L								E		E		L					L
X0X1	R			E									E							E	L								
X101	R				E									E						E				L	E				
X111	R					L									L						L		E		E		L		
X1X1	R						E									E						E	E	L				
XX01	R																			E							L	E
XX11	R								L									L			L			L		E		E
XXX1	R																					E				E	L	

FIG. 6

	I, Q +	0001	0011	0101	0111	1001	1011	1101	1111
I-, Q									
0001	R		L			E			
0011	R	E			L		L		
0101	R	E			L			E	
0111	R		L	E					L
1001	R	E					L	E	
1011	R		L			E			L
1101	R			E		E			L
1111	R				L		L	E	

FIG. 7

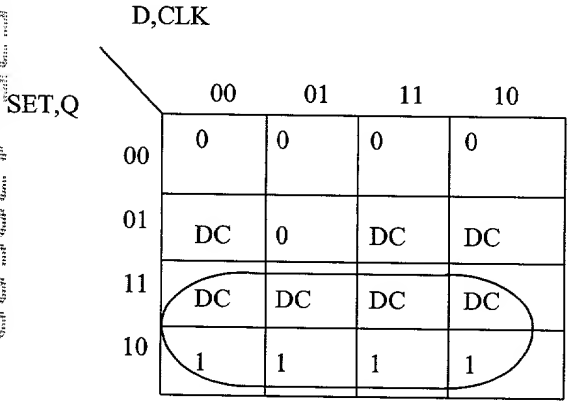

FIG. 8

SET,Q	D = 0	D = 1
00	0	1
01	0	1
11	DC	1
10	DC	DC

FIG. 9

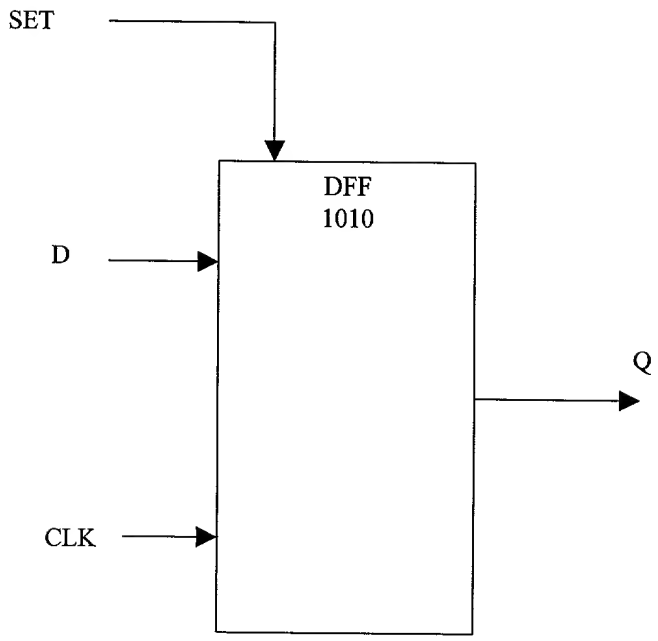

FIG. 10

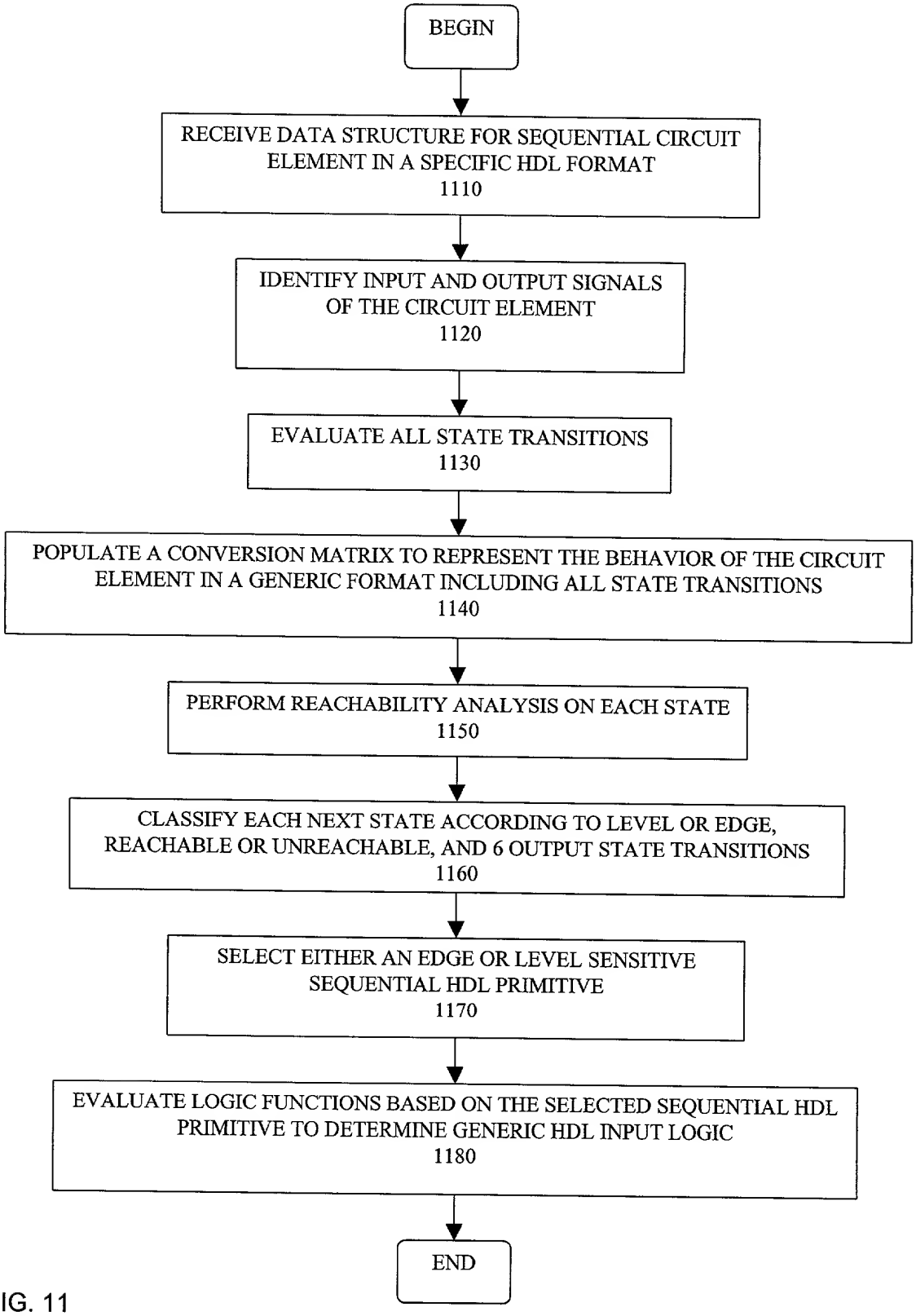
BEGIN
RECEIVE DATA STRUCTURE FOR SEQUENTIAL CIRCUIT ELEMENT IN A SPECIFIC HDL FORMAT
1110
IDENTIFY INPUT AND OUTPUT SIGNALS OF THE CIRCUIT ELEMENT
1120
EVALUATE ALL STATE TRANSITIONS
1130
POPULATE A CONVERSION MATRIX TO REPRESENT THE BEHAVIOR OF THE CIRCUIT ELEMENT IN A GENERIC FORMAT INCLUDING ALL STATE TRANSITIONS
1140
PERFORM REACHABILITY ANALYSIS ON EACH STATE
1150
CLASSIFY EACH NEXT STATE ACCORDING TO LEVEL OR EDGE, REACHABLE OR UNREACHABLE, AND 6 OUTPUT STATE TRANSITIONS
1160
SELECT EITHER AN EDGE OR LEVEL SENSITIVE SEQUENTIAL HDL PRIMITIVE
1170
EVALUATE LOGIC FUNCTIONS BASED ON THE SELECTED SEQUENTIAL HDL PRIMITIVE TO DETERMINE GENERIC HDL INPUT LOGIC
1180
END

FIG. 11

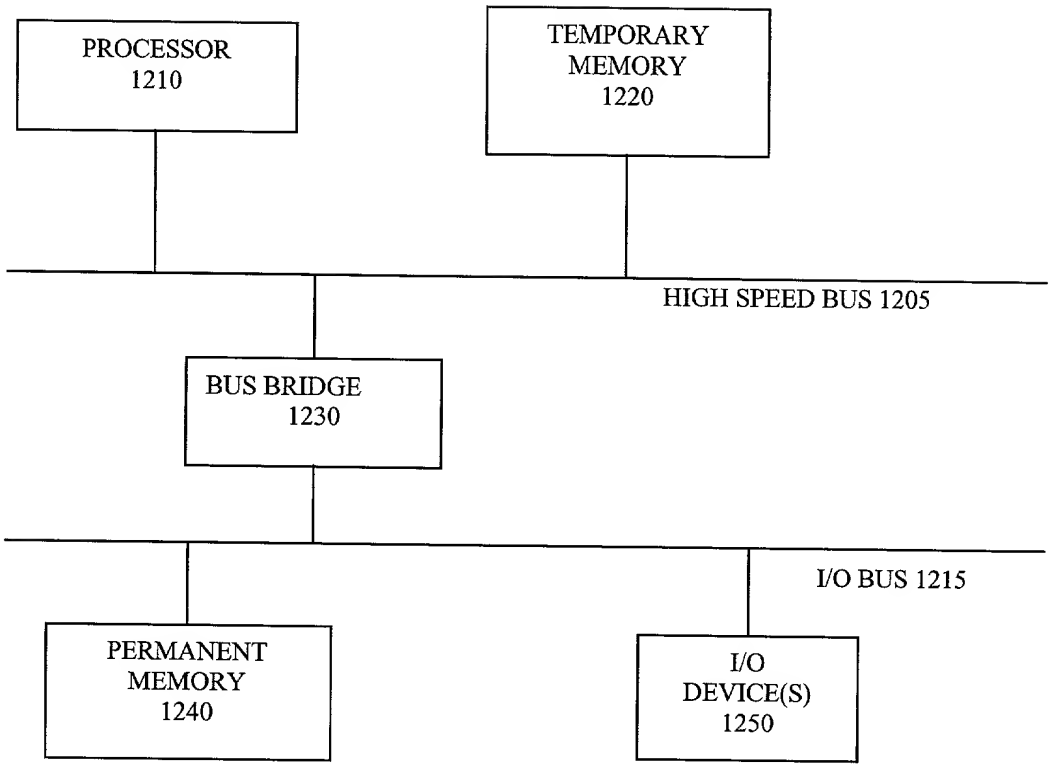
PROCESSOR
1210
TEMPORARY
MEMORY
1220
HIGH SPEED BUS 1205
BUS BRIDGE
1230
I/O BUS 1215
PERMANENT
MEMORY
1240
I/O
DEVICE(S)
1250

FIG. 12

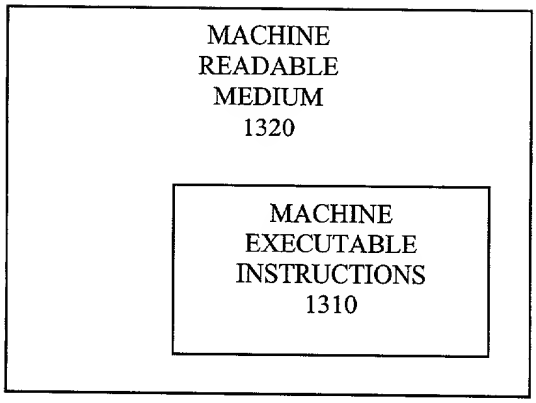
MACHINE
READABLE
MEDIUM
1320
MACHINE
EXECUTABLE
INSTRUCTIONS
1310

FIG. 13